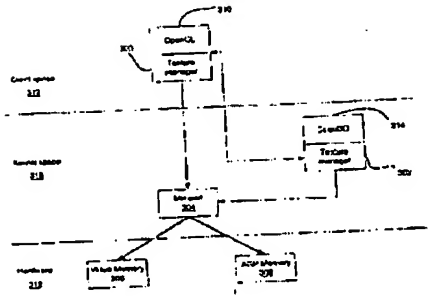
REMARKS

The Examiner rejected Claims 1-29 under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (US2002/0101427A1), hereinafter "Nguyen." Applicant respectfully disagrees with this assertion.

Specifically, the Examiner now relies on the following excerpts from Nguyen to make a prior art showing of applicant's claimed "sending an instruction request to memory utilizing a texture module in a graphics pipeline" and "receiving instructions from the memory in response to the instruction request utilizing the texture module in the graphics pipeline." See this or similar language in each of the independent claims.

> [0025] The processes of the present invention are performed by processor 202 using computer implemented instructions, which may be located in a memory such as, for example, main memory 204, memory 224, or in one or more peripheral devices 226-230.
>
> [0032] The process begins by receiving a request to store a texture in texture memory (step 400). A texture is reloaded as needed (step 402). Texture memory is then allocated to the current texture in the request (step 404). In this example, the allocation occurs through a call made by the texture manager to a miniport or other memory allocation mechanism. A determination is made as to whether the allocation was successful (step 406). In this example, allocations are done a per mipmap basis. A texture object consists of one or more mipmaps starting from level 0 and the allocation always begins with mipmap 0, then 1, and so on. A mipmap is a reduced resolution version of a texture map, used to texture a geometric primitive whose screen resolution differs from the resolution of the source texture map.
>
> [0036] The removed texture is marked (step 412). If a texture is removed from APG memory, this texture is marked as a APG texture such that when it is reactivated or loaded again, this texture will be loaded into APG memory. If the texture is removed from video memory, it is marked as a video texture so that this texture will be reloaded into video memory the next time it is requested for use. Memory is allocated to the current texture object (step 414) with the process then returning to step 406 as described above.

Figure 3



After carefully reviewing such excerpts and the remaining Nguyen reference, applicant respectfully asserts that the Nguyen is no more pertinent than the Migdal reference, which was previously relied upon by the Examiner.

Specifically, at best, Nguyen discloses that main memory 204 includes both instructions and textures (by virtue of including APG memory 308 managed by the texture manager 300). However, applicant respectfully asserts that no texture module in Nguyen (i.e. texture manager 300, etc.) in any way sends instruction requests for receiving instructions from memory. After carefully reviewing the Nguyen reference, it is clear that every texture-related module merely submits texture requests for receiving texture data, *not* instructions.

Thus, it is clear that, similar to the previous Migdal reference, Nguyen fails to disclose, teach or even suggest any sort of "sending an instruction request to memory utilizing a texture module in a graphics pipeline" and "receiving instructions from the memory in response to the instruction request utilizing the texture module in the graphics pipeline" (emphasis added).

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical

invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

This criterion has simply not been met by the Nguyen reference. Specifically, only applicant teaches and claims sending "instructions requests" and retrieving "instructions" in the specific context of "utilizing a texture module." By retrieving the instructions utilizing the texture module, much pipeline bandwidth is saved at the input of the texture module, since prior art configuration data at least in part need not necessarily be received from the rasterizer. Moreover, memory traditionally employs a high-bandwidth connection with the texture module, which may be used for efficient retrieval of the instructions.

The instructions may then be used by the texture module in order to control various graphics processing involving the texels, pixels, and/or primitives, etc. For example, the instructions may control how subsequent texels may be mapped to pixels associated with primitives. Moreover, the instructions may be used to control the mapping, or blending, of the texels with the pixels, in accordance with the instructions. Simply nowhere in the prior art is there such a combination of features for fulfilling the foregoing objectives.

Applicant further emphasizes that the Examiner's application of Nguyen to applicant's remaining claims is replete with deficiencies.

Just by way of example, applicant claims in dependent claims that "the instructions are adapted for controlling a texture environment module coupled to the texture module" (see Claim 6). The Examiner relies on the following excerpt from Nguyen to show such feature in the prior art.

> [0025] The processes of the present invention are performed by processor 202 using computer implemented instructions, which may be located in a memory such as, for example, main memory 204, memory 224, or in

one or more peripheral devices 226-230.

After a careful review of such excerpt, applicant contends that this excerpt is lacking, especially in view of the shortcomings of the Examiner's application of Nguyen to the independent claims. For example, the abovementioned "processor" does not include a "texture module," as claimed by applicant. Only applicant teaches and claims sending "instructions requests" and retrieving "instructions" "utilizing a texture module" which provides the aforementioned advantages that are non-existent in the prior art including Nguyen.

Similarly, the Examiner relies on the following excerpt from Nguyen to make a prior art showing of applicant's claimed "initial instructions [that] control at least the sending of the instruction request by the texture module" (see Claim 9), "a complete instruction set [that] is received in response to the instruction request" (see Claim 18), and "a partial instruction set [that] is received in response to the instruction request" (see Claim 19).

> [0032] The process begins by receiving a request to store a texture in texture memory (step 400). A texture is reloaded as needed (step 402). Texture memory is then allocated to the current texture in the request (step 404). In this example, the allocation occurs through a call made by the texture manager to a miniport or other memory allocation mechanism. A determination is made as to whether the allocation was successful (step 406). In this example, allocations are done a per mipmap basis. A texture object consists of one or more mipmaps starting from level 0 and the allocation always begins with mipmap 0, then 1, and so on. A mipmap is a reduced resolution version of a texture map, used to texture a geometric primitive whose screen resolution differs from the resolution of the source texture map.

Once again, there is simply no mention in the excerpt above of any sort of instruction retrieval utilizing a texture module, let alone "initial instructions [that] control at least the sending of the instruction request by the texture module," "a complete instruction set [that] is received in response to the instruction request," and "a partial instruction set [that] is received in response to the instruction request," as claimed by applicant.

Again, the aforementioned anticipation criteria has simply not been met by the Examiner's reference. A specific prior art showing of such claim limitations or a notice of allowance is respectfully requested. All of the pending independent claims are thus deemed allowable along with any claims depending therefrom.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. For payment of any fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP064/P000286).

Respectfully submitted,

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